REMARKS

Claims 1-18, 21 and 22-24 are pending. By this Amendment, claims 10, 12 and 13 are amended and claims 23 and 24 are added. Claims 14-18 and 22 stand allowed. The Office Action objects to claim 6 as dependent on a rejected base claim, but claim 6 otherwise specifies patentable subject matter. Claims 1-5, 7-13 and 21 stand rejected. Claim 23 specifies the subject matter of claim 1 and includes features specified in claims 5 and 6. Although dependent on claim 23, claim 24 specifies the subject matter of claim 2 and includes features specified in claims 5 and 6.

1. The Office Action rejects claims 12, 13 and 22 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With regard to claim 12, the Office Action asserts that the "specification does not disclose the CMOS circuitry process type well is formed to a greater depth than a depth of the first well as recited in claim 12." With regard to claim 13, the Office Action asserts that the "specification does not disclose the CMOS circuitry process type well is formed to a greater concentration than the second concentration as recited in claim 13." If applicable to the amended claims 12 and 13, these assertions, and the corresponding rejections, are respectfully traversed. The specification (e.g., page 9, lines 16-19) discloses an alternative embodiment where an extra implant process is used to increase the depth and/or dose of the p implant beneath the photodiode to increase the barrier, if needed.

With regard to claim 21, the Office Action asserts that the "specification does not disclose an epi layer of the first conductivity type in a second concentration, the second concentration being less than the first concentration; a first well of a second conductivity type formed in the epi layer as recited in claim 22." The Office Action asserts that page 9, lines 5-15 of the specification just refers to FIGS. 1, 2 and 3. To the contrary, page 9 of the specification at line 5 describes the paragraph ranging from line 5 to line 15 as an alternative embodiment, an alternative to the embodiment depicted in FIGS. 1, 2 and 3. However, much of the same structure from FIG. 1, 2 or 3 is carried into the alternative embodiment such as the p well barrier (e.g., p-region 14, 44 or 74 in FIG. 1, 2 or 3).

2. The Office Action rejects claims 10-13 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action asserts that it is unclear whether the "CMOS process type well" recited in claims 10, 12 and 13 as "the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type" refers to first well 74 of FIG. 3. If applicable to the present claims, this assertion, and the corresponding rejection is respectfully traversed. As specified in the claims, the sensor includes CMOS circuitry to control the sensor and a first well formed in the substrate. Then, the CMOS circuitry is further specified to include a CMOS well and at least one FET formed in the CMOS well. Thus, it is clear that the CMOS well and the first well are distinct.

3. The Office Action objects to the drawings under 37 C.F.R. § 1.83(a) for failing to show every feature of the invention specified in the claims. A Request For Approval Of Drawing Corrections is hereby attached to conform the drawings to the specification. It is respectfully submitted that this Request obviates the objections to the drawings. No new matter is added.

4. The Office Action rejects claims 1 and 7-11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,448,104 to Watanabe. For at least the reasons discussed herein, withdrawal of these rejections is respectfully solicited.

Watanabe does not disclose a sensor that includes both CMOS circuitry and photodiode region formed in a first well as specified in claims 1 and 10, and therefore specified in all claims dependent thereon.

The Office Action cites FIGS. 10A, 10B and 10C of Watanabe and asserts that the CMOS circuitry to control the sensor, as specified in claims 1 and 10, is disclosed as circuitry 3. This assertion is respectfully traversed.

Since circuitry 3 includes only a single transistor, it cannot constitute CMOS circuitry. The Office Action admits (lines 1 and 2 of page 5) that CMOS circuitry requires an n-channel FET and a p-channel FET. FIGS. 10A, 10B and 10C of Watanabe does not disclose both an n-channel FET and a p-channel FET as required to constitute the CMOS circuitry specified in claims 1 and 10.

Watanable does not disclose any relationship between CMOS circuitry and the device depicted in FIGS. 10A, 10B and 10C. Watanable does not discloses a sensor that includes both CMOS circuitry and photodiode region formed in a first well as specified in claims 1 and 10. "The identical invention must be shown in as complete detail as is contained in the ... claims." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). See also M.P.E.P. section 2131. Therefore, Watanable cannot be said to anticipate claims 1 and 7-11 under 35 U.S.C. § 102(e). Withdrawal of the rejections of claims 1 and 7-11 under 35 U.S.C. § 102(e) is respectfully solicited.

5. The Office Action rejects claims 2-5 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,448,104 to Watanabe in view of U.S. Patent No. 6,297,070 to Lee, et al. For at least the reasons discussed herein, withdrawal of these rejections is respectfully solicited.

The Office Action again cites FIGS. 10B and 10C of Watanabe and asserts that the CMOS circuitry to control the sensor is disclosed as circuitry 3. For at least the reasons discussed above with respect to the rejections of claims 1 and 7-11, this assertion is respectfully traversed.

Furthermore, the Office Action fails to establish a *prima facie* case that claims 2-5 would have been obvious to a person of ordinary skill in the art. In particular, the Office Action fails to take into consideration teachings of Watanabe. A prior art reference must be considered in its entirety including portions that would lead away from the claimed invention. See *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Also see M.P.E.P. section 2141.02. In addition, the modification proposed by the Office Action would render the Watanabe device unsatisfactory for its intended purpose. Watanabe describes, in FIG. 10, a passive pixel sensor. As taught by Watanabe (column 3, lines 1-13), to reduce the dimensions of the transistors and maintain transistor performance, the p implant concentration has to be increased, and this results in a decreased thickness of the depletion region and a consequential reduced sensitivity to photons. But Watanabe notes that enhancement of the sensitivity of the photo detector can be most efficiently achieved by expanding the area of the depletion layer (column 2, lines 56-58). Thus a tradeoff is established. Watanabe teaches that the photodiode is formed directly on the substrate. See FIGS. 1, 2, 3, the deep depletion layer in

FIG. 4). See also column 4, lines 37-51 and claim 1, lines 4-7. The teaching of Watanabe is that in order to increase sensitivity, the photodiode is formed on the substrate with no barrier p well between. Insertion of a p well between would render the device unsatisfactory for Watanabe's purpose. In fact, Watanabe teaches that the removal of this p-implant beneath the photosite is for the purpose of removal of any barrier to charge generated more deeply in the silicon as a means of increasing sensitivity (FIG. 1, column 7, lines 55-65) to longer wavelength light. In contrast, the present invention teaches that the electrical p-well implant of the CMOS circuitry can also be used to form a barrier.

"The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)." See M.P.E.P., section 2143.01, page 2100-98, Rev. 1, Feb. 2000, 7th Ed (emphasis in the original). Watanabe teaches removal of a p implant beneath the photodiode. This achieves greater sensitivity in the Watanabe device. Imposing the p implant again would be unsatisfactory for Watanabe's intended purpose. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)." See M.P.E.P., section 2143.01, page 2100-99, Rev. 1, Feb. 2000, 7th Ed (emphasis in the original).

Accordingly, it would not have been obvious to modify Watanabe, even with the teachings of Lee, et al. to achieve the present invention.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Prompt reconsideration and allowance are earnestly solicited. Should the examiner believe that any further action is necessary to place the application in condition for allowance, the examiner is invited to contact the under signed at the telephone number listed below.

Respectfully submitted,

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